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EXAMINER

KERVEROS, JAMES C

ART UNIT PAPER NUMBER

2133

10

DATE MAILED: 06/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/020,200

Applicant(s)

LAVIE ET AL.

Examiner

James C Kerveros

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 01 March 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☒ Claim(s) 1-14 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 March 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

1. Claims 1-21 are pending and are hereby presented for examination.

***Claim Objections***

2. Claims 1-14 are objected to because of the following informalities:

Claims 1, 8 and 5, 12, line 8 and line 2, respectively, the word "remain" should be inserted before the word "unchanged".

Claims 4, 11, line 2, the word "and" should be deleted, because of a typographical error. Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3-7, 10-14 and 17-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 3 and 10 recite the limitation of "wherein ordering the flip-flops is dependent upon the type of device being scanned", which renders the claim indefinite, because the term "ordering the flip-flops" represents terminology inconsistent with accepted meaning.

Claim 17 recites the limitation of "synchronize the transmission of the contents of the proud to flip-flops over the scan chain signal", which renders the claim indefinite,

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because the term "proud" is improper terminology and does properly describe the synchronization function.

Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "ordering the flip-flops" in claims 3 and 10 is used by the claim to mean "clocking the flip-flops", while the accepted meaning is for example "ordering food". Also, the term "proud" in claim 17 is used by the claim to mean "plurality of flip-flops", while the accepted meaning is for example "proud person". Both terms "ordering" and "proud" are indefinite because the specification does not clearly redefine the term.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Chung et al. (US 6446230).

Regarding independent Claims 1, 8, 15, Chung discloses a method and apparatus for testing integrated circuit devices (ICs) according to (IEEE) standard 1149.1, comprising:

Transmitting an external event trigger signal, (b\_capture, FIG. 6A) from the compliance enabler (504) to a scan module (scan cell, 502-1) to begin a scan operation in the IC device 500A, (FIG. 5A). In the first preferred embodiment, scan cell (502, FIG. 5A) is shown in FIG. 6A as scan cell 601, which receives one signal or a combination of signals including external event trigger (b\_capture) signal.

Transmitting a synchronous scan command signal, such as (sys\_clk) on line 6003, to a device core (internal scan cell, 612) located inside core logic 304 of the DUT IC device 500A, where the (sys\_clk) is received from the functional system clock signal, TCK of enabler 504, which clocks flip-flop 610 during boundary scan testing and synchronizes its internal TAP controller 702 (FIG. 7A) with TAP controller 306.

When the synchronous scan command (b\_capture) signal is received by the device core internal scan cell (612) of core logic 304, the holding values stored in flip-flop 610 remain unchanged until the (sys\_clk) signal clocks the flip-flop

Transmitting the values (i\_sdo) of the output of flip-flop (610) on line 6023 to external test equipment (conventional ATE) through TAP controller (306, FIG. 5A), when the synchronous scan command signal (sys\_clk) is received.

Regarding Claims 2, 9, 16, Chung discloses an IEEE standard 1149.1 Test Access Port (TAP) controller 306, for connecting the external test equipment to the external event trigger signal and a scan chain signal. FIG. 7B shows the scan signals (TDI, TRST, TMS, TCK, and TDO) embedded in a baseboard (DUT 804), which includes for illustrative purposes, three chips (804-2, 4, 6) and boundary-test connector 8048, where the chips correspond to device IC device 500A, in FIG. 5A.

Regarding Claims 3, 10, 17, Chung discloses transmitting (*i\_sdo*) values using serial (*sys\_clk*) to shift the values from flip-flop (610) to the external test equipment (conventional ATE) via scan cells IEEE standard 1149.1 TAP controller 306, FIG. 5A.

Regarding Claims 4, 11, 18, Chung discloses receiving the values contained in the plurality of flip-flops (610) serially by the external test equipment (conventional ATE) via TAP controller 306, storing the values contained in the plurality of flip-flops in a memory system inherently located in the external test equipment, and reporting to a user through a display unit the values contained in the plurality of flip-flops.

Regarding Claims 5, 12, 19, Chung discloses synchronizing the plurality of flip-flops 610 in the device core logic 304 using a scan clock signal (*sys\_clk*) received from the functional system clock signal, TCK of enabler 504, which clocks flip-flop 610 during boundary scan testing and synchronizes its internal TAP controller 702 (FIG. 7A) with TAP controller 306.

Regarding Claims 6, 13, 20, Chung discloses Scan TCK signal, which is an external clock, controls the transmission timing of the values (*i\_sdo*) of the plurality of flip-flops being serially transmitted by the clock to the external test equipment.

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Regarding Claims 7, 14, 21, Chung discloses IC device 500A, (FIG. 5A), comprising a communications interface such as IEEE standard 1149.1 Test Access Port (TAP) controller 306.

**Conclusion**

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE  
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Date: 10 June 2004  
Office Action: Non-Final Rejection

By: 

James C Kerveros  
Examiner  
Art Unit 2133

  
for

Albert DeCady  
Primary Examiner